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APPLICATION N	0.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/611,547		07/02/2003	Jun Yamaguchi	116428	4984	
25944	7590	04/04/2005		EXAMINER		
		DGE, PLC	LEVI, DAMEON E			
P.O. BOX ALEXAN		VA 22320		ART UNIT	PAPER NUMBER	
	,			2841		
	•			DATE MAILED: 04/04/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

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		Application No.	Applicant(s)	
		10/611,547	YAMAGUCHI ET A	L.
Office Actio	n Summary	Examiner	Art Unit	
		Dameon E. Levi	2841	
The MAILING DA Period for Reply	TE of this communication	n appears on the cover sheet wi	th the correspondence add	lress
THE MAILING DATE OF - Extensions of time may be avail after SIX (6) MONTHS from the - If the period for reply specified a - If NO period for reply is specifie - Failure to reply within the set or	THIS COMMUNICATION The provisions of 37 CF is a communication of 38 CF is a communica	R 1.136(a). In no event, however, may a r	eply be timely filed by (30) days will be considered timely. ITHS from the mailing date of this considered timely. ANDONED (35 U.S.C. & 133).	nmunication.
Status				
1) Responsive to cor	nmunication(s) filed on	07/02/2003 New Application.		
2a) This action is FINA	AL . 2b)⊠	This action is non-final.		
		owance except for formal matt		merits is
closed in accorda	nce with the practice und	der <i>Ex parte Quayl</i> e, 1935 C.D	. 11, 453 O.G. 213.	
Disposition of Claims				
4)⊠ Claim(s) <u>1-20</u> is/a	re pending in the applica	ation.		
4a) Of the above c	laim(s) is/are with	ndrawn from consideration.		
5) Claim(s) is/	are allowed.			
6)⊠ Claim(s) <u>1-20</u> is/aı	•			
7) Claim(s) is/	are objected to.			
8) Claim(s) ar	e subject to restriction a	nd/or election requirement.		
Application Papers				
9)☐ The specification is	objected to by the Exa	miner.		
10) The drawing(s) file	d on <u>02 <i>July 2003</i></u> is/are	: a)⊠ accepted or b)⊡ objec	ted to by the Examiner.	
		the drawing(s) be held in abeyan		
		πection is required if the drawing(R 1.121(d).
		e Examiner. Note the attached		
Priority under 35 U.S.C. §	119			
12) Acknowledgment is	s made of a claim for for	eign priority under 35 U.S.C. §	119(a)-(d) or (f)	
	* c)⊠ None of:	oigh phonty under do d.c.c. 3	113(a)-(a) 01 (1).	
	•	nents have been received.		
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		list of the certified copies not	received	
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Attachment(s)				
1) Notice of References Cited (I	PTO-892)	4) Interview S	ummary (PTO-413)	
2) 🔲 Notice of Draftsperson's Pate	ent Drawing Review (PTO-948	Paper No(s)/Mail Date	
3) Information Disclosure Stater Paper No(s)/Mail Date	ment(s) (PTO-1449 or PTO/SE		formal Patent Application (PTO-	152)
· -po. rectopristal Date	•	6) 🔲 Other:	- ·	

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DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Wakabayashi et al US Patent 6560115.

Regarding claim 1, Wakabayashi et al discloses a module comprising:

a heat radiating member(for example, see element 60, Figs 1,2A, 2B, element 21, Fig 15) including a circuit arrangement surface having a circuit arrangement region a power circuit section(for example, see element 61, Figs 1,2A, 2B, element 6,7, Fig 15); including at least one electronic part and arranged in the circuit arrangement region;

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a wall member(for example, see element 54, Figs 1,2A, 2B, element 2, Fig 15); surrounding the circuit arrangement region;

and a resin layer (for example, see element 102, Figs 1,2A, 2B) disposed in a space defined by the wall member and the heat radiating member, wherein:

the electronic part has a plurality of leg portions(for example, see element 101, Figs 1,2A, 2B); and the resin layer seals least the leg portions(for example, see column 10, lines 40-42).

Regarding claim 2, Wakabayashi et al discloses further

comprising: a seal member surrounding the circuit arrangement region(for example, see elements 22, 23, Figs 15), wherein: the wall member defines a first groove to which the seal member is fitted(for example, see groove in element 2, 22, 23, Figs 15), and the seal member is interposed between the wall member and the heat radiating member.

Regarding claim 3, Wakabayashi et al discloses wherein the power circuit section includes at least one bus bar; the wall member includes a hood; and an end portion of the bus bar is inserted into the hood(for example, see column 9, lines 43–65).

Regarding claim 4, Wakabayashi et al discloses the wall member further includes a through hole communicating a side of the heat radiating member and a side of the hood; and a part of the bus bar passes through the through hole(for example, see elements 68,68C,54,80, Figs 10A-11B).

Regarding claim 5, Wakabayashi et al discloses wherein: the wall member further includes: a recess portion; and another through hole communicating the side of

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the heat radiating member and the recess portion(for example, see elements 66,66C,54,80, Figs 10A-11B).

Regarding claim 6, Wakabayashi et al discloses wherein: the bus bar has: a first portion extending in parallel with the circuit arrangement surface; and a second portion standing up from the circuit arrangement surface and inserted into the hood(for example, see elements 41,37,35 Fig 7).

Regarding claim 7, Wakabayashi et al discloses wherein: the wall member defines a second groove; the bus bar has: a first portion extending in parallel with the circuit arrangement surface; a second portion standing up from the circuit arrangement surface; and a third portion extending through the second groove(for example, see elements 42,39, Fig 7, elements 42, 79A, 79B, Fig 8).

Regarding claim 8, Wakabayashi et al discloses wherein the bus bar protrudes from at least one of side edges of the power circuit section in outward directions (for example, see elements 66,68, Fig 10A-11B).

Regarding claim 9, Wakabayashi et al discloses further comprising: an insulating layer disposed between the heat radiating member and the power circuit section(for example, see layer between elements 60 and 61, Fig 1)

Regarding claim 10, Wakabayashi et al discloses wherein the insulating layer is thermally connected with the heat radiating member and the power circuit section(for example, see layer between elements 60 and 61, Fig 1)

Regarding claim 11, Wakabayashi et al discloses further comprising: a lid attached to the wall member to cover the power circuit section(for example, see element 50, Fig 1).

Regarding claim 12, Wakabayashi et al discloses further comprising a bus bar constitution plate including a plurality of bus bars, wherein: the electronic part is electrically connected to the power circuit section and at least one of the bus bars(for example, see elements 51,52, Fig 1).

Regarding claims 13-20, the methods discloses therein are deemed inherent in the assembly of the claimed apparatus since the elements used for facilitating the methods are taught and suggested in the prior art of record. The claims are thus subsequently rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dameon E. Levi whose telephone number is (571) 272-2105. The examiner can normally be reached on Mon.-Fri. (9:00 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner Art Unit 2841

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